SAFE CONNECT SYSTEMS

Changing the game for reliable data architectures of Critical Systems

TSN

TSN Full Deterministic Switched End System for IOs & CPU

IP Core
1 interface with CPU
Scalable Up to 14 User IO Functions
Scalable Up to 23 Ports (1G/10G)

For Factory Automation, Automotive, Aerospace, Railways …

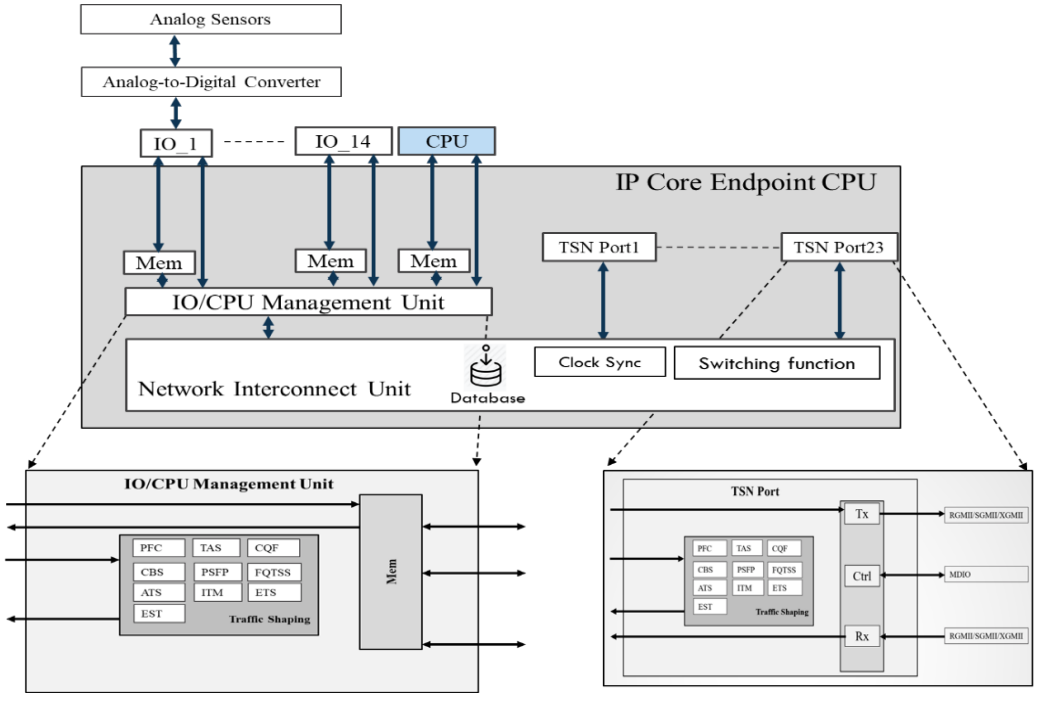
- Full hardware design
- Very small Footprint
- Highest operational performances
- Highest level of Safety certifiable hardware
- Maximum security against intrusions
- Reduce drastically costs

Overview

Safe Connect Systems (SCS) IP Cores allow to design full deterministic TSN critical applications with a full range of undisputed assets:

- TSN stack full hardware powerful implementation that reaches undisputed Performances such as Node synchronization accuracy, Switch traversal time, Ultra-Low Latency and Effective Bandwidth allocation.
- This implementation simplifies End User system design and reduces drastically development and recurring costs:
  - Very Easy, flexible and reliable Hardware interfacing
  - Very easy application integration
  - Functionally Extensible with end user HDL application code
  - Entirely Customizable: ports, memory, routing table
  - Strong level of integration with smart sensors or actuators
- This implementation of the TSN Stack is fully deterministic
  - Supports any TSN scheduler
  - Provides deterministic best (BCCT) and worst (WCCT) case communication time
  - Provides a very short time gap between BCCT and WCCT
  - Makes simple the demonstration of qualification for safety critical applications
- Considering its very small Footprint so that the IP Core can be onboarded on a large range of chips.
- Several internal powerful mechanisms for maximum security against intrusion.
- A set of additional value-added services over TSN that are simply accessible for the end user in order to reduce drastically the development of critical applications. These services reduce also drastically the recurring cost by minimizing the additional hardware required to monitor the critical system.

Block Diagram



TSN Features

 **Time Synchronization** • IEEE 802.1AS & 802.1AS-Rev Time GPTP Synchronization. • +/- 12ns Jitter for 1Gbps Link and 250 MHz internal frequency. • Grandmaster capability	 **Traffic Shaping** • IEEE 802.1Qav / Credit Based Shaping **(CBS)** •IEEE 802.1Qch /Cyclic Queuing and Forwarding **(CQF)** • IEEE 802.1Qcr Asynchronous Traffic Shaping **(ATS)** • IEEE 802.1Qbv enhancement for Scheduled Traffic: Time-Aware Shaper (**TAS**)	 **Reliability** • IEEE 802.1Qci Per-Stream Filtering and Policing **(PSFP)** • IEEE 802.1Q Forwarding and Queuing Enhancements for time Sensitive Stream **(FQTSS)** • IEEE 802.1Q Priority based Flux Control **(PFC)** • IEEE 802.1Q Enhanced Transmission Selection **(ETS)**

Features

Ports	• Scalable from 1 to 23 ports
One CPU Interface	• Easy CPU interface based on dual port shared memory
IO User VHDL functions	• Scalable from 1 to 14 IO functions with shared dual port memory interfaces
Speed	• 100/1000 Mbit/s; 10G Available 2020
Physical Interfaces	• RGMII, SGMII, XGMII (on demand)
Target Devices	• Arria10, Cyclone 10, Cyclone V, others on demand
Advised Boards	• Cyclone V SoC Multi-Port Ethernet Aggregator Board – NetLeap (4 ports) • Intel Cyclone 10 GX FPGA Development Kit (4 ports) • Arria 10 FPGA FMC Attila Instant-Development Kit for 4 ports; SCS extension for additional ports is available on demand
Net Bandwidth allocation	• up to 75%
Synchronization accuracy	• Synchronization accuracy < 20 ns (1 Gbps link)
Switch traversal time	• <2 µs for 23 ports EndSystem CPU/IO with typical frames
Footprint	• Minimal footprint per Communication Port: ALM < 5000; registers < 8000, Memory < 65 kbytes
Low power (FPGA & ASIC)	• Range of 1 Watt for one 4 ports end system node on FPGA
Available topologies	• Tree, point to point, ring, daisy chain • Combination of above
Verification	• The TSN-End System has been rigorously verified, hardware-validated, and tested in real-life environments.
Safety certifiable hardware	• Up to Dal A/ASIL-D/SIL4
Configuration	• Configuration tool and user guide
Added Value services	• Health Monitoring • Hardware based native seamless Redundancy • Security based services • Hardware Virtualization services (no external CPU required for network monitoring)
TSN Applications	• up to the most demanding applications including full determinism, very accurate synchronization, very short cycle time such (< 50 µs) such as motor control, medical machine, and/or very high traffic use such as vehicle backbone, critical video capture and monitoring, …
Deliverables	• Encrypted Qsys IP component • Test benches • Examples of reference design • Technical documentation • Getting started Guide
Tools	• Intel Altera based evaluation platform
Support	• The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.
Expertise	• SCS experts can also provide ad hoc consulting on demand about the design of critical systems distributed architectures